In the specification:

Please replace the paragraphs on lines 5-24 of page 1 and the paragraphs on lines 1-12 on page 2 of the patent application with the following.

U.S. patent application serial number 10/045,795 by T.B. Berg et al. (BEA919990003US1) entitled "Method And Apparatus For Increasing Requestor Throughput By Using Data Available Withholding" was filed on January 9, 2002.

U.S. patent application serial number 10/045,927 by T.B. Berg et al. (BEA920000017US1) entitled "Method And Apparatus For Using Global Snooping To Provide Cache Coherence To Distributed Computer Nodes In A Single Coherent System" was filed on January 9, 2002.

U.S. patent application serial number 10/045,821 by T.B. Berg et al. (BEA920000018US1) entitled "Multi-level Classification Method For Transaction Address Conflicts For Ensuring Efficient Ordering In A Two-level Snoopy Cache Architecture" was filed on January 9, 2002.

U.S. patent application serial number 10/045,797 by T.B. Berg et al. (BEA920000020US1) entitled "Method And Apparatus For Multi-path Data Storage And Retrieval" was filed on January 9, 2002.

U.S. patent application serial number 10/045,923 by W.A. Downer et al. (BEA920000021US1) entitled "Hardware Support For Partitioning A Multiprocessor System To Allow Distinct Operating Systems" was filed on January 9, 2002.

U.S. patent application serial number 10/045,925 by T.B. Berg et al. (BEA920000022US1) entitled "Distributed Allocation Of System Hardware Resources For Multiprocessor Systems" was filed on January 9, 2002.

U.S. patent application serial number 10/045,926 by W.A. Downer et al. (BEA920010030US1) entitled "Masterless Building Block Binding to Partitions" was filed on January 9, 2002.

U.S. patent application serial number 10/045,774 by W.A. Downer et al. (BEA920010031US1) entitled "Building Block Removal From Partitions" was filed on January 9, 2002.

U.S. patent application serial number 10/045,796 by W.A. Downer et al. (BEA920010041US1) entitled "Masterless Building Block Binding To Partitions Using Identifiers And Indicators" was filed on January 9, 2002.

Please replace the paragraph on lines 2-3 of page 6 with the following paragraph.

Figs. 1A and 1B ~~is~~ together form a logic diagram illustrating the operation of the apparatus and the method of the preferred embodiment of the invention.

Please replace the two paragraphs on lines 15-26 of page 8 and on lines 1-4 of page 9 with the following paragraphs.

Figs. 1A and 1B illustrate[[s]] the logic architecture and the process used in the preferred embodiment. A current transaction **62** is measured against the transaction look-up table **56** providing a standard output 77 as a preprogrammed response to the specific transaction. In the embodiment as shown in **Figs. 1A and 1B**, the current transaction **62** is also introduced into

comparator **58** at input **95**. Comparator **58**, if enabled through bit **72**, allows comparison of current transaction information input at **95**, with information provided to the comparator at input **94**.

Transaction identifier register (TIR) **50** is a software register designed to store the identification of those transactions identified in transaction look-up table **56** to provide a response that was unexpected or undesirable as the chip containing transaction look-up table **56**. There may be a variety of different transactions that, during the testing stage, have been identified as transactions of a certain identification **63**, length **64**, attribute **65** or target address **66** for which it is desired that the response originally programmed in transaction look-up table **56** should be altered to a redefined response which is more desirable. Such identified transactions are loaded in TIR **50**, and are communicated to transaction mask register (TMR) **52** which, as can be seen in **Figs. 1A and 1B**, parallel the definitions of the fields shown in TIR **50**. TMR **52** is comprised of a field for the transaction identifiers **67**, the length **68**, attribute **69** and target **70**, similar to the fields shown in TIR **50**.

Please replace the two paragraphs on lines 18-26 of page 10 and on lines 1-14 of page 11 with the following paragraphs.

The logic diagram illustrated on **Figs. 1A and 1B** will now be used to provide an example of the operation of the preferred embodiment. TIR **50** is shown in the diagram with binary code below each field which would be used in the example. Transaction field **63** is loaded with the binary transaction identifier 10110. TMR **52** has its transaction field **67** switched to 11111. Since field **67** and TMR **52** have their bits all selected on, or enabled, the transaction identifier in field **63** will be passed through TMR **52** exactly as presented, and transaction identification **90** shown

at 59 will appear unchanged from the transaction identifier in field 63. Moving to TIR 50 length at field 64, the bits entered in the example are 100. Since TMR 52 has 000 selected in its length field 68, the result of field 68 operating on field 64 is a "don't care" as depicted by common nomenclatures shown at 91 at 59. Accordingly, it will be appreciated that the transaction identified in TIR 50 at field 63 can be of any length in field 64 and not be further filtered or expanded by any operation of TMR 52 because its length field 68 has none of its enabled to further operate on field 64.

Continuing with the example shown in Figs. 1A and 1B, TIR 50 is showing the transaction attribute field 65 of value 000. TMR 52 has its attribute field 69 selected at 100. The results of the operation require the first bit of field 65 to be conveyed at 69 as shown at 92. However, since the remaining two bits of field 69 are set at 0, it can be seen that the results in the next two bits at 92 is a "don't care" condition. Accordingly, any transaction with a leading bit attribute at field 65 will meet the criteria to be selected, the next two bits in field 65 will not make a difference in the identified transaction to be redirected. Continuing with the example, the target field 66 in TIR 50 uses an example field of 1000. Field 70 of TMR 52 has its four bits all enabled, that is selected to 1111 thereby requiring that the resultant output at field 93, at 59 is conveyed exactly as presented in field 66.

Please replace the two paragraphs on lines 10-26 of page 12 and on lines 8-18 of page 13 with the following paragraphs.

While three different registers are shown for the purpose of describing the operation of the preferred embodiment, it can also be appreciated that there may be one physical register that may be designed to perform the functions of TIR 50, TMR 52 and TRR 54 without being separate

physical devices or registers. The entire method and system may be contained in a logic device which performs the operations of TIR **50**, TMR **52** and the comparator **58**. Further, more than one set of registers can be applied to the same lookup table to allow for adding or correcting more than one lookup table entry. It will be evident to those skilled in the art that the entire process may be carried out in one or more specialized components which perform essentially the same functions as the logic illustrated in **Figs. 1A and 1B**. The implementation of the design presented will depend on the complexity of look-up table **56** in a particular system, as well as the register size limits for the technology being used to implement the preferred embodiment described.

TIR **50** can also include response fields. For example, a field within TIR **50** which indicates whether a system had a hit on a address conflict queue can be included as a condition for redirection, even though such a field may relate to a different type of lookup structure as compared to the disclosure above describing the preferred embodiment. Adapting the invention to this alternative structure, for example, a redirected response would be presented if a certain response to the specified transaction occurs. Other such similar uses for the invention will be evident to those skilled in the art. Moreover, while the logic diagram in **Figs. 1A and 1B** discloses one way to utilize the invention, other logic structures which carry out the functions which are described in the disclosure will also be apparent to those skilled in the art. Such alternate means to carry out the invention are considered to be within the scope of the parent invention which fully encompasses such other embodiments.